Cost-Effective Built-In Test for Advanced Aircraft Electrical Systems

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This paper presents a method for utilizing the data handling portion of the Advanced Aircraft Electrical System (AAES) to provide a cost-effective built-in test capability to isolate faults to the line replaceable unit (LRU). The evolved techniques provide a means for determining the health of each of the 2048 input and 2048 output controls (signal transducers and power switches) that are multiplexed by the system. The system also automatically tests the integrity of all the aircraft electrical distribution system signal and power wire, terminations, and connector pins. Four techniques to automatically test the data handling and multiplex circuits are also discussed. The built-in test (BIT) system as defined is efficient, small in size and weight, fully automatic, and cost-effective because most of the data and test circuits are time-shared to accommodate BIT data. The BIT data can be used inflight in power management equation solutions to permit programming of redundancy and safety interlocks. Two maintenance displays are discussed: a maintenance panel and an onboard strip printer. The BIT system is compatible with an air-to-ground data link of maintenance data. Also discussed are techniques for manufacturing and field checkouts of the system and wiring during manufacture and after field modifications.

Introduction

MAINTAINABILITY has been a prime consideration during the development of the Advanced Aircraft Electrical System by Vought.[1,2] As a result of this concern, several new built-in test (BIT) techniques have been evolved and demonstrated as an integral part of the system; these techniques add very few parts to the system while improving system performance and life cost. These techniques can be utilized in other multiplex systems with similar improvements. The abbreviation BIT is used instead of BITE because the techniques do not add an appreciable amount of built-in test equipment.

In a conventional aircraft electrical power system, the power is routed through a circuit breaker, then through a series of switches and relays. However, in the new system, known as SOSTEL (Solid State Electric Logic), all control signals and logic are handled at the signal level by a unique multiplex system as shown in Fig. 1.

All input control signals are derived from low-power-level single-pole devices called signal sources. For the developed system, up to 64 signal sources can be connected to each multiplex terminal. This information is multiplexed to the processor where system logic is performed. Output information is transmitted to demultiplexers that control solid-state power controllers. Utilization power is obtained directly from the bus through the load controllers to each respective load. The processor and transmission lines are redundant. The multiplexers and demultiplexers are internally redundant.

This paper shows that the maintainability objectives can be met with very little increase in the number of onboard circuits when they are integrated into the system as part of the initial design requirements. Furthermore, the result is improved inflight characteristics and lower life-cycle costs.

Maintenance Objectives

The maintenance objectives were established by an analysis of the needs of the maintenance personnel–what information is needed to correct each malfunction. The major problems of flight-line personnel, especially on the aircraft carrier flight deck, are[3]: short turnaround time, availability of ground power, communication with flight personnel, poor lighting (night adaption red), space limitation, and radio silence. The BIT system must, therefore, provide sufficient failure data display without requiring external electrical power and be readable in all ambient lighting levels.

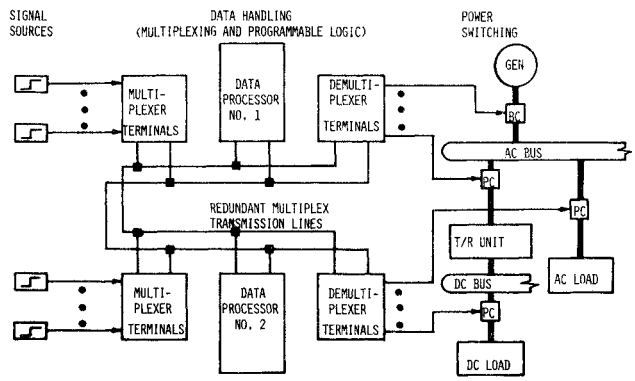

Fig. 1 SOSTEL distribution system block diagram.

A major portion of flight-line maintenance personnel's time is spent in trouble-shooting and preparing report forms.[4] Automatic isolation to the line replaceable unit (LRU) level will eliminate most of the trouble-shooting time; also, this program examined ways to do the recording chore for the flight-line personnel.

After the LRU is removed from the aircraft, maintenance personnel must then identify and replace the appropriate throwaway module. The method of providing this access must be established during the planning stage. Adding BIT checkout capabilities used only on the bench was discussed by Bucher.[5] "A major pitfall with BITE, however, is that the typical designer tends to go overboard: The designer wants to fly the intermediate shop-test equipment as well as the flight line equipment." ". . . fault isolation capability at any specific level of maintenance should provide only the capability to isolate trouble to the unit or assembly that is replaceable at this level."

The additional access needed by bench-test personnel to isolate a failed subassembly should be provided by in-

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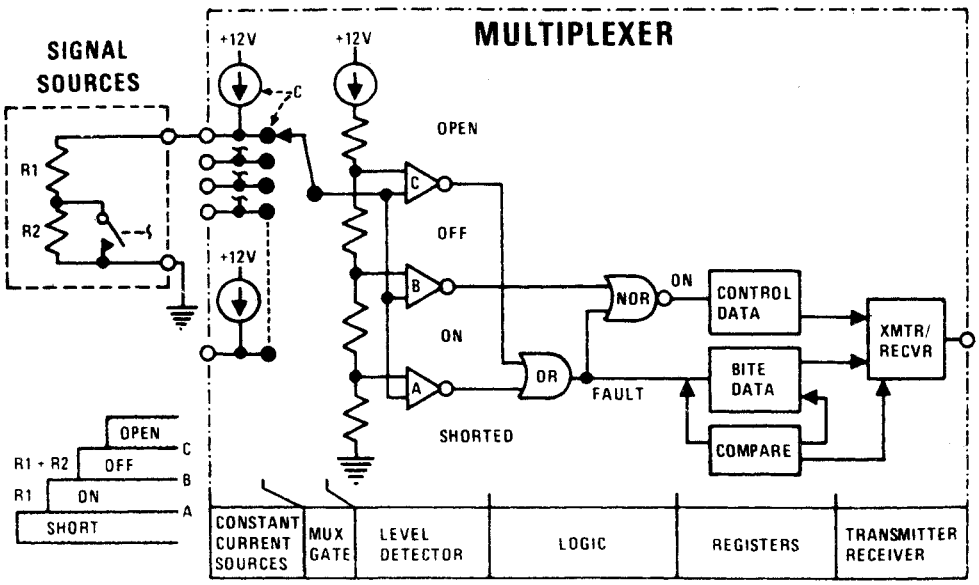

Fig. 2 Switched impedance signal source.

corporating test points. BIT will help bench-test personnel by virtually eliminating the removal of good equipment. Furthermore, BIT can reduce the problems of poor report data and erratic faults by designing the system such that the failure information is kept with the equipment when the equipment is removed from the aircraft. Therefore, BIT can be a major benefit to bench-test personnel without adding any onboard components especially for their benefit.

With these maintenance objectives in mind, the next step is to discuss BIT techniques for detecting malfunctions.

Signal Source Wire and Wire Termination Faults

To detect wiring faults between the multiplexer and the signal source (switch), there must be a way to distinguish between a broken wire and an open switch, and between a shorted wire and a closed switch. After considering numerous approaches, the simplest technique was determined to be the switched impedance concept functionally illustrated in Fig. 2. Four impedance bands were established which are SHORT, ON, OFF, and OPEN. Normally the resistance changes between R1 and R1 + R2 for ON and OFF states, respectively. Fault modes exist when the impedance value is below or above the normal values; that is, a SHORT or an OPEN.

The switched impedance approach not only provides sensing of wiring and certain types of signal source faults, but also provides additional advantages. It reduces the number of wires to each signal source (switch). The state of the signal sources can be pulse sampled thereby providing a significant power savings. The signal source can be smaller, more reliable. Because of the large quantity of signal sources (up to 2048) in the SOSTEL system, these simplifications also provide a significant cost savings. Note that existing switches can easily be converted to this approach by simply adding two resistors.

Signal Source/Multiplexer Interface

To detect the impedance, the multiplexer can be arranged to supply a constant current to the signal source. The resultant voltage levels are proportional to the impedance levels. The basic operation of the signal source/multiplexer interface is shown in Fig. 3.

Constant current sources are shown for each input; however, experience has shown that proper operation can be attained by pulsing the constant current source ON only during the sampling interval. This type of control provides a signal source power reduction of 500-to-1 as compared to previous approaches.

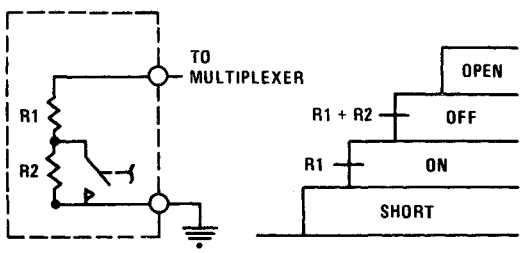

Fig. 3 Signal source/multiplexer interface.

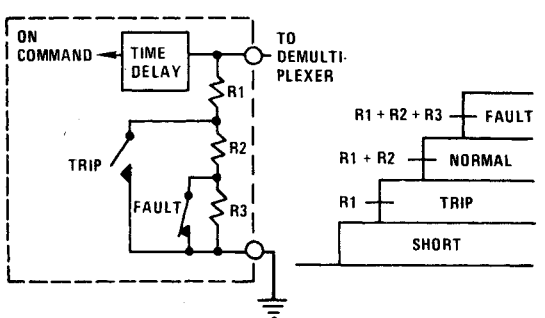

Fig. 4 Solid-state power controller input functional schematic.

The level detector uses reference voltages developed by a constant current source that provides very close tracking with the other current sources over a wide range of variations in temperature and line voltage. The level detector, including the operational amplifiers and the two logic gates, are time-shared; therefore, there are very few parts added for these BIT functions.

Load Controller and Signal/Power Wiring Faults

The solid-state load controllers provide the functions of power switching and circuit protection. To expand the BIT fault detection to include load controllers and related wiring requires that the system detect faults in the control wiring, power wiring, and the controller.

The switched impedance concept can also be applied to the power controllers with minor modifications, but with even greater savings. The wiring between the demultiplexer and power controller must communicate—commands from the demultiplexer (ON/OFF and RESET) to the power controller, and status data (tripped and faulted) from the controller to the demultiplexer.

This can all be accomplished with one line between the demultiplexer and power controller by using the switched impedance approach shown in Fig. 4. The same four impedance bands are used except that they represent SHORTED, TRIPPED, NORMAL, and FAULT. A fault indication from the power controller is defined as either an ON command with no output current (an open controller), or an OFF command with output current (a shorted controller).

Based on this definition, the fault-sensing circuit internal to the power controller will sense: 1) an open power controller, 2) an open wire from the power controller to the load, 3) a dead bus, 4) a shorted controller, or 5) a faulted controller circuit. In addition, a.c. power controllers have a serious failure mode of half-wave operation. This failure mode can be detected by using a current transformer that will saturate and provide the same indication as "no output current."

A short delay time of 100 μsec was included in the control circuit to permit testing the controller in the OFF state without actuating the power controller. The delay also serves the function of a noise filter. The "tripped" indication is arranged to override the "fault" impedance change. This prevents an offsetting impedance change, which might occur if "fault" increased the impedance and then "trip" lowered it by a similar amount. Trips imply a short circuit on the load side of the power controller; therefore, the power controller must latch until reset by removing the control signal. This may be implemented by using an SCR for the "trip" switch. On the other hand, "faults" are defined as the inability of the controller to respond to commands. If the ability is restored, the fault indication should automatically revert to normal; therefore, the "fault" switch should not be a "latch"-type function.

By the above discussion, one might get the impression that the BIT circuit adds complexity; however, operational breadboards have been built that demonstrated all the characteristics discussed with fewer and lower cost components than previous approaches.

Power Controller/Demultiplexer Interface

The power controller/demultiplexer interface is very similar to the signal source/multiplexer interface. There are three functional areas where they differ.

First, the impedance steps represent SHORTED, TRIPPED, NORMAL, and FAULTED, respectively, instead of SHORTED, ON, OFF, and OPEN. Second, the constant current source output must be ON continuously, rather than pulsed, when the power controller is commanded to be ON; therefore dedicated constant current sources must be used for each output and power dissipation will be higher than in the multiplexer. Third, the status of the controller is monitored when the controller is commanded to be ON by sensing the voltage level at the demultiplexer output. The health of the controller is also monitored in its off state by pulsing the constant current gate ON for 50 μsec.

Communicating Fault Data to the Processor

To communicate the basic power management data, the multiplex system operates at 1 MHz and is MIL-STD-1553 compatible. The BIT data collected per frame potentially doubles the communication load. Therefore, new techniques were developed to transmit the BIT data without significantly affecting the bit rate. The technique of transferring signal source fault data from the multiplexer to the central processor is based on the following five criteria. First, BIT data are transmitted only when a change in BIT status has occurred. This criteria was established to avoid serious impact on the system data rate. Second, BIT data are transmitted instead of input control data when a change is detected. Therefore, no unique time slot is needed in the communication frame for BIT data. Third, BIT data are transmitted before the respective input control data. This provides the central processor the opportunity to preserve the last valid update of channels with failed signal sources. Fourth, BIT data are transmitted if a faulted signal source returns to normal. The data is transmitted in this case to remove the inhibit of the channel. Last, BIT data continue to be transmitted by the multiplexer until the processor acknowleges the transmission. This guarantees that the BIT message is not lost.

The technique for transferring power controller trip and fault data from the demultiplexer to the central processor is different from the multiplexer reporting because the demultiplexer normal function is to receive control data from the processor. Unlike the multiplexer, it does not have a dedicated time slot to report the detail status of each power controller. Also, the demultiplexer may have any combination of trips and faults to report, and the data inhibit capability is not applicable for power controllers BIT data as it was with the signal sources. Because of these differences, the demultiplexer only reports that it has some "trip(s) and/or fault(s)" during the normal report cycle. This alerts the central processor to readdress the demultiplexer to get the detail trip or fault report during one of the spare message times at the end of the normal polling sequence.

Detecting Multiplex System Faults

The SOSTEL system uses four additional test techniques for ensuring the validity of the data used (data security) and detecting equipment malfunctions. The first two are common in multiplex systems and discussed here only briefly.

Address/Response

The processor transmits a unique address to the remote terminal. Only one terminal can recognize this address and responds by repeating the address. The processor checks the address in the return message against the address it transmitted.

Parity

One bit is reserved at the end of each data word for parity. The type of parity used examines mid-bit transitions of the biphase manchester code to detect invalid data. If parity does not check, the message is rejected. If two successive messages are rejected, the appropriate terminal is transferred to the redundant side.

Pump Up

Before a demultiplexer will change the status of a load controller from either OFF to ON or ON to OFF, it must receive the same change instructions in two successive frames of data. Therefore, it is extremely unlikely that noise will affect the same bits on two successive messages.

Circulating Test Bit

The processor generates a BIT source, which is sent out to all terminals each frame. It is sent to the multiplexers in the control word. It is then sent out on one pin of the signal source input connector and back in on another pin. This bit is then returned in a designated data channel. It is sent to the demultiplexer terminals in a designated data channel and returned in the demultiplexer status word. The processor uses these same BIT source bits to checkout all operations of the logic processor. By circulating the BIT source bit through each multiplexer and demultiplexer on a dedicated data channel as well as through the logic equation solution, a verification is obtained that the complete data system is operating correctly.

Maintenance Display

The maintenance display for the SOSTEL system must be capable of recording and displaying any combination of 6276 possible faults:

Input faults	2048
Output faults	2048

Output trips	2048
Terminals (4 × 2)	128
Processors	2
Transmission lines	2

Data must not be lost if power is removed; therefore, nonvolatile storage is required to insure the availability of data for the postflight BIT data display. Nonvolatile storage of BIT data can be implemented by a number of techniques, such as flag type indicators, nonvolatile memories, photographs, punches, recorders, and printers. These techniques were investigated and two are used in the maintenance panel and another in the maintenance printer which is discussed in a following section.

Maintenance Panel

The maintenance panel for the SOSTEL system must not only be capable of recording the displaying fault data, it must also contain controls to exercise the redundant parts of the multiplex system. The maintenance panel also serves as an interface between the maintenance personnel and the multiplex system to permit power controllers to be turned off or prevented from turning on for performing aircraft maintenance.

The maintenance panel developed for the SOSTEL data handling system was configured to display data handling system LRU faults on the left-hand side of the panel. Indicators were provided to denote the faulted portion (primary and secondary side) of redundant LRU's. The data handling system units can be forced to either primary or secondary operation, by means of switches on the maintenance panel to ensure that faults in the secondary units will be detected and reported. The remainder of the panel was dedicated to the display of BIT and control data for the multiplexer and demultiplexer channels.

The BIT data for the data handling system and all its input and output channels are stored in nonvolatile memory during the system operation and are available for display on the panel when the panel display is activated. All fault data are stored in memory including momentary or intermittent faults. These data are retained in memory until the memory is reset via the maintenance panel controls.

An onboard maintenance panel must be small and lightweight. To display all 2048 inputs and outputs for the system would require an excessively large maintenance panel display. To achieve the small size and weight requirements, the fault data were displayed one terminal at a time. Since multiplexer and demultiplexer terminal has 64 channels, the BIT data are stored in memory in 64 bit blocks corresponding to the terminal. The panel then displays the terminal number and the terminal input and output data for that terminal. The terminal number display is an LED type two digit numerical display. The channel status is displayed on an array of 64 (4 rows by 16 columns) LED's.

The maintenance panel has three modes of operation associated with the terminal number and channel displays. The first mode displays BIT (fault and trip) data, which is the primary function of the panel. The second mode displays the current input and output data for the system. The third mode is used for the command inhibit of the demultiplexer outputs (power controllers).

BIT data can be displayed either automatically or manually. In the manual mode, the BIT memory is scanned for faults. Each time a fault indication is detected in memory, the data for the terminal containing the fault is displayed. On command from the maintenance personnel, the automatic scan is continued. This process continues until all the faults (or trips) have been displayed. In the manual mode, the terminals are selected by number and the data displayed for the selected terminal.

The display of current input and output data is accomplished only using the manual mode. In this case, a terminal number is selected via thumbwheel switches on the panel and the current ON-OFF status of each channel of that terminal is displayed.

The inhibit mode works similar to the other two manual display modes except in this case only outputs can be inhibited. The inhibit mode is similar to opening a circuit breaker in a conventional aircraft power system. In this case, it is done electronically by selecting, by number, the demultiplexer and the channel to be inhibited and then activating the inhibit set switch. This action will turn the power controller off if it is on and prevent it from being turned on when it is off. The inhibit is removed by selecting the inhibited terminal and channel number and activating the inhibit reset switch. It can also be removed by activating the all inhibit reset switch. This switch resets all inhibits at one time. The inhibit status can also be displayed on the channel display. All control functions of the maintenance panel are disengaged when the access door is closed. The maintenance panel provides all of these functions in considerably less space than would be required for a circuit breaker panel.

Printer

The addition of an *onboard* printer operated under the control of the SOSTEL system yields a major improvement in the display of maintenance data. The requirements of storing and recording of fault data are met by a small, strip printer.

An onboard printer provides several advantages over the maintenance panel. It eliminates the need for nonvolatile memory storage of BIT data, for ground or aircraft power to readout fault data, and for manually transcribing failure data. The printer provides a "hard copy" of failures to accompany the failed LRU's. The printer also improves the accuracy and confidence in failure data. The printer can also provide a time base and sequence of events for more accurate failure analysis. The ASC II Alpha-Numeric print capability may be useful in recording maintenance data for other computer-controlled systems. The printer being onboard instead of being a piece of support equipment is the key factor in most of the above advantages and also eliminates the need for flight-line support equipment for the SOSTEL system.

The printer is controlled to print each time a failure is sensed. Therefore, repeated entries indicate an erratic failure.

Continuous recording of flight data typically requires an elaborate recorder and the addition of extensive wiring.[6] However, this printer can actually provide continuous recording for the 6276 possible faults. Furthermore, capacity can be provided to include fault recording for other airplane systems, yet provide a more easily understood hard-copy output than other onboard data recorders, which provide miles of records but have less channel capacity.

Data Link (Air to Ground)

The printer interface is easily adaptable to a data link system so that fault data can be transmitted to a base station. This allows extensive use of ground-based computer facilities for failure analysis, identification of spare parts so that maintenance personnel can have parts ready when the plane lands, and for locating spare parts so that the flight can be diverted to where spares are available to reduce aircraft down time. For further information on the potential of data link for aircraft maintenance refer to C-5A literature on MADAR.[7]

Inflight System Improved by BIT

The BIT techniques discussed in this paper provide several improvements in the inflight system which include significant power reductions, no system disturbance by a switch failure, programmable automatic corrective action, and reduced flight crew workload.

When a switch failure is detected, this fact is transmitted to the processor before the input control data and is used to inhibit the update of that channel. The last valid data con-

tinues to be used for logic solution. Therefore, a switch failure will not cause a change in the aircraft characteristics. The flight crew can also be immediately notified of the failure. For situations where a failure requires immediate corrective action, the BIT data can be included in the logic to provide automatic corrective action thereby reducing flight-crew workload.

Simplified Wiring Checkout

When aircraft wiring is installed or modified, the electrical system must be checked out to assure that wiring installation is correct. This checkout determines if the wiring has shorts or opens and if it is connected to the correct terminals.

The checkout of aircraft wiring is presently a tedious and time-consuming procedure of actuating combinations of switches and observing various outputs. The SOSTEL/BIT system can be used to simplify this operation and reduce the time required to establish that the wiring is not open or shorted and that each signal source is connected to the correct multiplex input pin.

A number of approaches can be used to accomplish this checkout task. For example, the processor can be loaded with a checkout program that sequences through the signal sources to detect crossed wires. When the operator actuates a designated signal source, the processor acknowledges by activating an indicator, then steps on to the next signal source. Power controllers can then be checked by temporarily programming the processor such that each power controller is controlled by one signal source that is convenient and in the proximity of the load. After the checkout is completed, the processor memory is loaded with the inflight program. This checkout approach does not require any additional support equipment and does not add any components to the flight system.

Test by the BIT system is better than conventional production and retrofit wiring test equipment because BIT continuously monitors all wiring for shorts and opens with the wiring in the flying location and connection. This approach locates more erratic faults than the conventional equipment and avoids wire and connector breakage, which is occasionally caused by connection and disconnection of the wiring test equipment. Time to accomplish wiring checkout with BIT is reduced, which can result in shorter production cycle and higher aircraft availability.

BIT checkout procedures may eliminate the following costs, which are normally associated with aircraft wiring checkout: 1) cost of test equipment to checkout the aircraft wiring, 2) labor cost of attaching, operating, and disconnecting the wiring test equipment, 3) cost resulting from damage, which occasionally occurs during attaching and disconnecting the wiring test equipment, 4) material and labor cost of onboard connectors normally added specifically to facilitate checkout of aircraft wiring, and 5) labor cost of troubleshooting wiring faults by eliminating faults in the test equipment wiring. These savings can appreciably offset the cost of incorporating the SOSTEL/BIT system.

Conclusion

The advanced BIT techniques discussed in this paper provide several ways of improving maintainability and reducing aircraft life cycle costs. These improvements include: 1) better and lower cost wiring checkout, 2) improved mission effectiveness and the mean-time-between maintenance-actions due to increased reliability, 3) reduction in spares requirements due to reduction in good component removals, 4) reduced maintenance manhours per flight hour (resulting from reduced MTBMA's, automatic identification of failed LRU's, and the use of the maintenance panel as an aid in system checkout), 5) fewer aircraft and support personnel required because of increased aircraft availability and mission effectiveness, and 6) lower equipment cost due to reduced flight-line support and intermediate level equipment. In addition, savings in power, space, and weight will also provide tangible benefits.

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